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REMARKS

In the first Office Action dated October 29, 2007, the Examiner rejected claims 1-16 and 37-40 under 35 U.S.C. 112 first paragraph as failing to comply with the written description requirement and under 35 U.S.C. 103 as obvious over the combination of DiStefano (U.S. Patent No 6,127,724) and Iijima (Japanese Patent Applications P2003-030767—U.S. counterpart Publication No. 2004/0155358.

Applicants have amended claims 1, 6, 10, 12, and 15 in response to the rejections. Claims 1-16 and 37-40 remain at issue. Support for amendment to claim 1 may be found at least at Figs 2 and 5; page 7, lines 26-28; page 11, lines 22-24; page 15, lines 28 to page 16, lines 2; page 16, lines 21 to 27. Amendments to claims 6, 10, 12, 15 are found in the original claims.

Written Description Rejections

Claims 1-16 and 37-40 were rejected as failing to comply with the written description requirement. Claims 1, 6, 10, 12, and 15 were previously amended to recite "active" and "non-active" surfaces instead of top and bottom surfaces of a die. In order to expedite prosecution, these claims are amended back to reciting "top" and "bottom." Applicants hereby requests withdrawal of this rejection because the claims no longer recite "active" and "non-active."

Art Rejections

Claims 1-16 and 37-40 were rejected as obvious over DiStefano and further in view of Iijima. Applicants respectfully submit that claim 1, the only independent claim, is not obvious over DiStefano and Iijima.

Claim 1 recites:

A semiconductor package comprising:

a die having a plurality of layers of low-K dielectric material in the die, the die having a top surface including circuitry fabricated thereon, a non-active surface *not including circuitry*, and a plurality of side surfaces, each surface having associated corner and edge regions;

a wire bonding packaging substrate having a plurality of electrical contacts, the packaging substrate being positioned under the die;

a plurality of interconnects electrically connecting the die to the plurality of electrical contacts;

a molding interface material applied to at least a portion of the top surface of the die, the molding interface material being configured to control at least one of tensile and shear stresses experienced by the die in the proximity of the active surface; and

a molding cap including a molding compound covering at least a portion of the die, packaging substrate, interconnects, and the molding interface material;

wherein the molding interface material is a *discrete layer* separate from the molding compound and formed between the molding cap and the die.

Claim 1 recites a semiconductor package having a die, a molding interface material on at least a portion of the top surface of the die, and a molding cap covering the molding interface material. Thus the molding interface material is *between the molding cap and the die.* Of particular note is that the molding interface material is a separate and a discrete layer separate from the molding compound in the molding cap. The specification discloses the relationship between the molding compound and the molding interface material in at least the following sections:

"The packages of the present invention include a *molding interface material* that is *applied between the* low-K Si *die and the molding compound* such that the molding interface material strengthens the structural integrity of the low-K Si die..." (specification page 7, lines 26-29, emphasis added)

"*molding interface material* also provides adhesion *between low-K Si die* 202 and the *molding compound of molding cap* 212 such that low-K Si die 202 is stably integrated within molding cap 212." (specification page 11, lines 22-24, emphasis added)

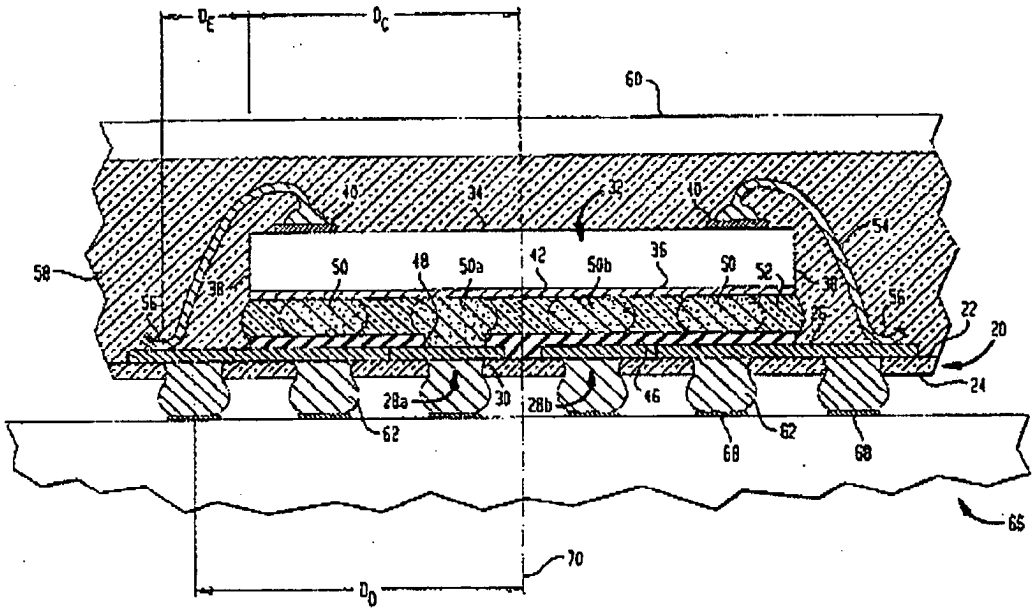
"Since some *molding compounds* have a high CTE relative to that of low-K Si die 502, a coat of *molding interface material 516 can be generally applied over low-K Si die* 502 to create a stress buffering *layer* (e.g., stress buffer zone; stress barrier) *there-between* so that stress from the molding compound does not fall directly onto low-K Si die 502." (specification page 15 line 28 to page 16 line 2, emphasis added)

DiStefano and Iijima do not disclose or suggest, singly or in combination, a structure where a separate layer of material is applied between a top surface of a die and the molding compound. The Examiner points to DiStefano Figure 1, element 52 as a molding interface material applied over a top surface of the die. For convenience purposes, Figure 1 from DiStefano is reproduced below. In discussing element 52, DiStefano discloses:

A flexible rear encapsulant 52 occupies the space between the rear surface 36 of the chip [32] and the top surface 22 of the dielectric layer [20], completely filling any voids left

unoccupied by the posts, insulating layer 46, and traces 26. (DiStefano, column 7, lines 51-54)

FIG. 1



As shown in the figure, the rear encapsulant 52 is located between a rear surface of the chip (32 in Figure 1 of DiStefano or 202 in Figure 2 of this application), and a top surface of the dielectric layer (20 in Figure 1 of Di Stefano or 204 in Figure 2 of this application). In fact the rear encapsulant 52 can be said to be equivalent to the die-attach adhesive of Figure 1A and 1B of this application.

The encapsulant 58 of DiStefano serves an equivalent purpose as the molding compound of the present application. DiStefano discloses for element 58 of Figure 1 shown above, "a dielectric lead encapsulant 58 intimately surrounds the leads or bonding wires 54 and covers the top surface 34 of the chip as well as the top surface 22 of the dielectric layer." (column 7, lines 56-59) The present specification discloses for molding compounds, "the molding compound is used to couple together the various components (e.g., electrical contacts, substrate, die attach pad, die, etc.) of the wire bonding package." (page 2, lines 6-9) Comparing the two statements, it is apparent that they both surround these various leads, wires, electrical contacts and cover the top surface of the chip or die. Claim 1 requires the molding interface material layer to be between the die and the molding compound. Thus, in order for rear encapsulant 52 to anticipate

the molding interface material of the present application, the rear encapsulant 52 must be placed between the lead encapsulant 58 and the chip.

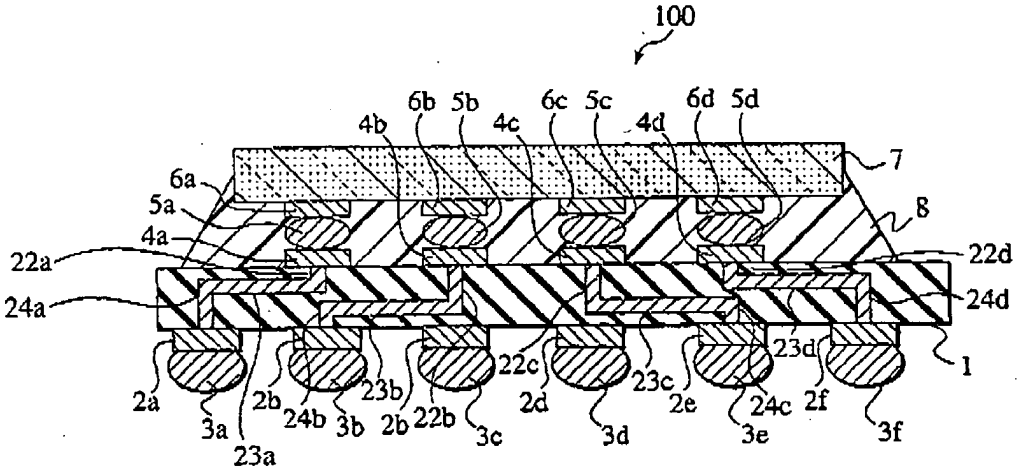
The Examiner also cites other parts of DiStefano to support the notion that encapsulant 52 is equivalent to the molding interface material of the present invention. Particularly, the Examiner cites Figure 7 and associated text on column 13. Applicants would like to point out that Figure 7 and associated text discuss the use of a spreader on top of an encapsulant 458. There is no disclosure of any layer between the encapsulant 458 and the die. Thus, the molding interface layer of the present application is not found any where in DiStefano.

The Examiner argues that the possible compositions recited in the application for the molding interface material and the encapsulant overlap because they are both available from Dow Chemical Company of Midland, Michigan. However, the "any suitable material" in the specification (see page 11) is followed by "can be applied to any surface ... of low-K Si die so that the package stress experienced by low-K Si die 202 is minimized to safe levels." Thus, any suitable material is not any material or any material produced by Dow Chemical Company, but only those that can minimize package stress when it is a part of the package as described in the application. Further, claim 1 requires that the molding interface material be a discrete layer from the molding compound. Assuming *arguendo* that the molding interface material has the same composition as the encapsulant of DiStefano, claim 1 still requires a discrete separate layer. DiStefano does not disclose two separate layers of encapsulants.

The rear encapsulant 52 is not applied to a top surface of the die and is not placed in between the encapsulant 58 and the chip. Therefore, rear encapsulant 52 of DiStefano cannot be a molding interface material as claimed.

The Examiner also point to Iijima Figure 1, element 8 as the molding interface material. As shown in Figure 1 (reproduced below for convenience) and disclosed in paragraph 24, element 8 is disposed in between chip 7 and substrate 1. Claim 1 of this application requires a molding interface material to be between the molding cap and the die. Iijima does not disclose a molding cap. If a molding cap is applied to the package of Iijima, it cannot be applied on the other side of element 8 from the chip 7, because the substrate 1 is there. Thus the element 8 in Iijima cannot be said to be between a molding cap and a die.

For at least the foregoing reasons, the molding interface material of claim 1 is not taught or suggested in DiStefano and Iijima, either singly or in combination. Because the molding interface material is not obvious over cited prior art, claim 1 and claims dependent therefore from are not obvious over cited prior art.



It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below. If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 500388 (Order No. ALTRP100).

Respectfully submitted,
BEYER WEAVER LLP

Jonathan O. Scott
Reg. No. 39,364

P.O. Box 70250
Oakland, CA 94612-0250
(510) 633-1100